
Features

- Serial Communication Controller
- Two Independent Full-duplex Channels
- Asynchronous and Synchronous Modes
- MONOSYNC, BISYNC and SDLC Loop Mode Supported
- SDLC Loop Mode Supported
- NRZ, NRZI and FM Encoding/Decoding
- Digital PLL for Each Channel
- Baud Rate Generator for Each Channel
- Local Loop-back and Automatic Echo Modes
- Gate Count: 11200 Gates

Introduction

The CB_82530 Macrocell is a serial communication controller with two independent full-duplex channels which support asynchronous, bit synchronous and byte synchronous communication modes. The CB_82530 is fully programmable by an 8-bit system interface. The interrupt controller has external signals that allow it to be daisy-chained with other interrupt controllers.

Each of the two channels of the CB_82530 contains a transmitter, a receiver, a baud rate generator, a digital phase-locked loop and a clock selector. The clock can be programmed to come from one of two external clocks, from the baud rate generator, or derived from the received data stream by the PLL. In addition to the two serial communication channels there is a common 8-bit system interface and a six-source interrupt controller.

In SDLC mode a zero insertion block will insert zeros into long strings of ones. A CRC generator produces a CRC check word for appending to message blocks. The final output selector allows the output to come from the receiver in diagnostic or loop modes.

The receiver input selector allows the received data stream to come from the transmitter in diagnostic modes or through a 1-bit delay, which is required in SDLC loop mode. The receive data shift register can be extended to 16-bits for detecting 16-bit sync characters, and can automatically delete the extra zeros that were inserted into the data stream in SDLC mode. A CRC checker can be used in synchronous modes.



Standard Interface Macrocell

CB_82530 Serial Communication Controller

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Signal description

Figure 1. Symbol

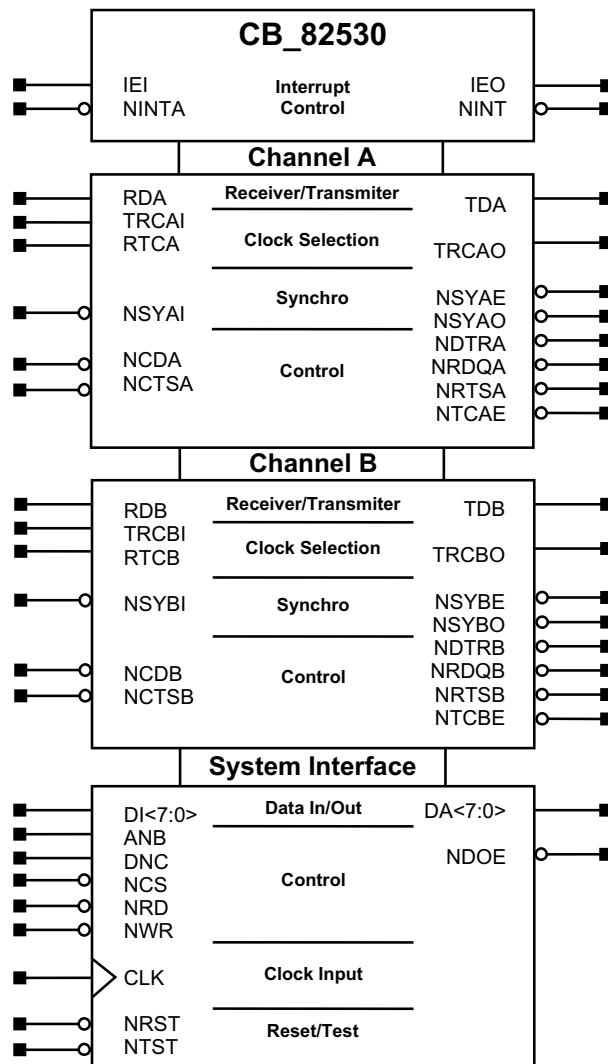


Table 1. Input Signals

Signal Name	Description
IEI	Interrupt enable in
NINTA	Interrupt acknowledge (active low)
RDA	Receive data, channel A
TRCAI	Transmit/Receive clock input, channel A
RTCA	Receive/Transmit clock, channel A
NSYAI	Synchronization in, channel A (active low)
NCDA	Carrier detect, channel A (active low)
NCTSA	Clear to send, channel A (active low)
RDB	Receive data, channel B
TRCBI	Transmit/Receive clock input, channel B
RTCB	Receive/Transmit clock, channel B
NSYBI	Synchronization in, channel B (active low)
NCDB	Carrier detect, channel B (active low)
NCTSB	Clear to send, channel B (active low)
DI<7:0>	Input data bus
ANB	A/B channel select (high=channel A)
DNC	Data/Command select (high=data)
NCS	Chip select (active low)
NRD	Read strobe (active low)
NWR	Write strobe (active low)
CLK	System clock
NRST	Reset (active low)
NTST	Test mode select (active low)

Table 2. Output Signals

Signal Name	Description
IEO	Interrupt enable out
NINT	Interrupt request (active low)
TDA	Transmit data, channel A
TRCAO	Transmit/Receive clock output, channel A
NSYAE	Synchro direction control, channel A (low=out)
NSYAO	Synchronization out, channel A (active low)
NDTRA	Data terminal ready/request, channel A (active low)
NRDQA	Ready/Request channel A (active low)
NRTSA	Request to send, channel A (active low)
NTCAE	Tx/Rx clock direction control, channel A (low=out)
TDB	Transmit data, channel B
TRCBO	Transmit/Receive clock output, channel B
NSYBE	Synchro direction control, channel B (low=out)
NSYBO	Synchronization out, channel B (active low)
NDTRB	Data terminal ready/request, channel B (active low)
NRDQB	Ready/Request channel B (active low)
NRTSB	Request to send, channel B (active low)
NTCBE	Tx/Rx clock direction control, channel B (low=out)
DA<7:0>	Output data bus
NDOE	Data bus direction control (low=output)